Claims

[c1] 1. A memory device structure, comprising:

a substrate;

a gate oxide layer disposed on a portion of the substrate;

a gate disposed on the gate oxide layer;

a buried bit line disposed in the substrate along both sides of the gate;

a raised line disposed on the buried bit line;

a spacer disposed on both sidewalls of the gate structure, thus isolating the gate and the raised line;

a word line disposed on the gate in a direction perpendicular to the buried bit line; and

an insulation layer disposed on a top of the raised line to electrically isolate the word line and the raised line.

[c2] 2. The structure as claimed in claim 1, wherein a material for forming the insulation layer comprises silicon oxide.

[c3] 3. The structure as claimed in claim 1, wherein a material for forming the spacer comprises silicon oxide.

[c4] 4. The structure as claimed in claim 1, wherein a material for forming the raised line comprises polysilicon.

[c5] 5. The structure as claimed in claim 1, wherein a material for forming the word line comprises polysilicon.

[c6] 6. The structure as claimed in claim 1, wherein the buried bit line is a shallow junction buried bit line.

[c7] 7. A method for forming a memory device, comprising:

forming a bar-shaped conductive structure on a substrate, wherein a cap layer is formed on a top surface of the bar-shaped conductive structure, while a gate oxide layer is formed underneath a bottom of the bar-shaped conductive structure;

forming a buried bit line in the substrate along both sides of the bar-shaped conductive structure;

forming a spacer on sidewalls of the bar-shaped conductive structure;

forming a raised line on the buried bit line;

forming an insulation layer on the raised line;

removing the cap layer;

forming a first conductive layer over the substrate to cover the bar-shaped conductive structure; and

forming a word line and a plurality of gates over the substrate by patterning the first conductive layer and the bar-shaped conductive structure in a direction perpendicular to the buried bit line.

[c8] 8. The method as claimed in claim 7, wherein there is a first etching selectivity between the cap layer and the spacer.

[c9] 9. The method as claimed in claim 7, wherein there is a second etching selectivity between the cap layer and the insulation layer.

[c10] 10. The method as claimed in claim 7, wherein a material for forming the cap layer comprises silicon nitride.

[c11] 11. The method as claimed in claim 7, wherein a material for forming the spacer comprises silicon oxide.

[c12] 12. The method as claimed in claim 7, wherein a material for forming the insulation layer comprises silicon oxide.

[c13] 13. The method as claimed in claim 7, forming the bar-shaped conductive structure further comprising:

forming a thin oxide layer, a second conductive layer and a material layer on the substrate sequentially;

patterning the second conductive layer and the material layer to form the bar-shaped conductive structure and the cap layer; and

removing the thin oxide layer that is not covered by the bar-shaped conductive structure, so that the remained thin oxide layer underneath the bar-shaped conductive structure is the gate oxide layer.

[c14] 14. The method as claimed in claim 7, wherein the method for forming the

insulation layer is a thermal oxidation process or a chemical vapor deposition method.

[c15] 15. The method as claimed in claim 7, wherein a material for forming the raised line comprises polysilicon.

[c16] 16. The method as claimed in claim 7, forming the raised line on the buried bit line further comprising:
forming a conductive material layer over the substrate; and
etching back the conductive material layer to expose the cap layer and a portion of the spacer, so that the remained conductive material layer is the raised line.

[c17] 17. The method as claimed in claim 7, wherein a material for forming the word line comprises polysilicon.

[c18] 18. The method as claimed in claim 7, wherein the buried bit line is a shallow junction buried bit line.